Objectives:

1. To evaluate the common-source amplifier using the small signal equivalent model.
2. To learn what affects the voltage gain.

Theory:

A self-biased n-channel JFET with an AC source capacitively coupled to the gate is shown in Figure 1-a. The resistor, $R_G$, serves for two purposes: it keeps the gate at approximately 0 V dc (because $I_{GSS}$ is extremely small), and its large value (usually several megohms) prevents loading of the ac signal source. The bias voltage is created by the drop across $R_S$. The bypass capacitor, $C_2$, keeps the source of the FET effectively at ac ground.

The signal voltage causes the gate-to-source voltage to swing above and below its Q-point value, causing a swing in drain current. As the drain current increases, the voltage drop across $R_D$ also increases, causing the drain voltage to decrease. The drain current swings above and below its Q-point value in-phase with the gate-to-source voltage. The drain-to-source voltage swings above and below its Q-point value 180° out-of-phase with the gate-to-source voltage, as illustrated Figure 1-b.

The operation just described for an n-channel JFET can be illustrated graphically on both the transfer characteristic curve and the drain characteristic curve in Figure 2. Figure 2-a shows how a sinusoidal variation, $V_{gs}$, produces a corresponding variation in $I_d$. As $V_{gs}$ swings from the Q point to a more negative value, $I_d$ decreases from its Q-point value. As $V_{gs}$ swings to a less negative value, $I_d$ increases. Figure 2-b shows a view of the same operation using the drain curves. The signal at the gate drives the drain current equally above and below the Q
point on the load line, as indicated by the arrows. Lines projected from the peaks of the gate voltage across to the $I_D$ axis and down to the $V_{DS}$ axis indicate the peak-to-peak variations of the drain current and drain-to-source voltage, as shown.

Small signal model of JFET is identical to that of the MOSFET in Figure 3. Here, $g_m$ is given by

$$g_m = \frac{2 I_{DSS}}{|V_p|} \left( 1 - \frac{V_{GS}}{V_p} \right)$$

or alternatively by

$$g_m = \frac{2 I_{DSS}}{|V_p|} \left( \frac{I_D}{I_{DSS}} \right)$$

where $V_{GS}$ and $I_D$ are the DC bias quantities, and

$$r_O = \frac{|V_A|}{I_D} \quad \text{and} \quad g_m \approx -2 \frac{I_{DSS}}{V_p}$$

At high frequencies, the equivalent circuit of Figure 4 applies with $C_{gs}$ and $C_{gd}$ being both depletion capacitances. Typically, $C_{gs}=1.3\pF$, $C_{gd}=0.1..0.5\pF$ and $f_t=20..100\ MHz$; and also there is a knowledge about the following:
\[ AV = \frac{gm(R_D // R_L)}{(1 + gmR_S)} \quad \text{(normally)} \]
\[ AV = \frac{gmR_d}{1 + gmR_S}, \quad R_d = \frac{R_D // R_L}{(RD // RL)} \]
\[ I_D = 2 I_{DSS} \left[ (R_{Sgmo} + 1) - (2R_{Sgmo} + 1)^{1/2} \right] / (R_{Sgmo})^2 \]

For the n-channel JFET current-voltage characteristics described as follows:

- **Cutoff**: \( V_{GS} \leq V_p, \quad i_D = 0 \)
- **Triode region**: \( V_p \leq V_{GS} \leq 0, \quad V_{DS} \leq V_{GS} - V_p \)
  \[ i_D = I_{DSS} \left( 2 \left( \frac{V_{GS}}{V_p} \right) \left( \frac{V_{DS}}{V_p} \right) - \left( \frac{V_{DS}}{V_p} \right)^2 \right) \]
- **Saturation region (pinch-off)**: \( V_p \leq V_{GS} \leq 0, \quad V_{DS} \geq V_{GS} - V_p \)
  \[ i_D = I_{DSS} \left( \frac{V_{GS}}{V_p} \right)^2 (1 + \lambda V_{DS}) \]

\( \lambda \) is the inverse of the Early voltage; \( \lambda = 1/V_A \). \( V_A \) and \( \lambda \) are positive for n-channel devices.

**Preliminary Work:** *(Choose and solve at least one question in each part –A,B,C-)*

Please use the formulae above!

A. Find the values of \( I_D, \quad V_{GS} \quad \text{and} \quad V_{DS} \) and find \( g_m \) in the circuit of Figure 7 then fill the Table 1 in the report to compare the measured ones.

B. In following questions 1 to 4, let the n-channel JFET have \( V_p = -4V \) and \( I_{DSS} = 10mA \), and unless otherwise specified assume that in pinch-off (saturation) the output resistance is infinite.

1. For \( V_{GS} = -2V \), find the minimum \( V_{DS} \) for the device to operate in pinch-off. Calculate \( i_D \) for \( V_{GS} = -2V \) and \( V_{DS} = 3V \).

2. For \( V_{DS} = 3V \), find the change in \( i_D \) corresponding to a change in \( V_{GS} \) from \(-2\) to \(-1.6V\).

3. For small \( V_{DS} \), calculate the value of \( r_{DS} \) at \( V_{GS} = 0V \) and at \( V_{GS} = -3V \).

4. If \( V_A = 100V \), find the JFET output resistance \( r_O \) when operating in pinch-off at a current of 1 mA, 2.5 mA and 10 mA.

C. 1. The JFET in the circuit of Figure 5 has \( V_p = -3V, \quad I_{DSS} = 9mA \), and \( \lambda = 0 \). Find the values of all resistors so that \( V_G = 5V, \quad I_D = 4mA \), and \( V_D = 11V \). Design for 0.05 mA in the voltage divider.
2. For the JFET circuit designed in question 6, let an input signal $v_i$ be capacitively coupled to the gate, a large bypass capacitor be connected between the source and ground, and the output signal $v_O$ be taken from the drain through a large coupling capacitor. The resulting common-source amplifier is shown in Figure 6. Calculate $g_m$ and $r_O$ (assuming $V_A = 100V$). Also find $R_{in}, A_V = v_O/v_i$, and $R_O$.

**Procedure:**

1. Construct the circuit in Figure 7:
2. Measure the values of $I_D$, $V_{GS}$ and $V_{DS}$ and find $g_m$ then fill the Table 1 in report part with your calculated values and compare the results.

3. With oscillator, obtain a 5 KHz signal with 0.5 Vpp and connect to the circuit as $V_{in}$, observe the $V_{out}$ signal and find the voltage gain.

4. Measure the AC voltage at source point of FET as $V_S$ and write some comments on this occurrence.

5. Reduce the $R_L$ and find the voltage gain.

6. Reduce the bypass capacitor and find the voltage gain. (**Never ask “which capacitor?”**)

7. Draw all graphs for $V_{in}$ and $V_{out}$, indicate the phase differences if they exist.

**Equipment List:**

- MPF102 FET transistor or equivalent
- DC power supply (15 V)
- Capacitors: 2*2.2 µF, 1*100 µF
- Resistors: 2*1 kΩ, 1*4.7 KΩ, 1*100 KΩ
- Oscilloscope

**References:**

- Microelectronic Circuits, Fourth Edition, Sedra&Smith, FET Small Signal Analysis
- Electronic Devices, Third Edition, Floyd, JFET Amplifiers
REPORT:

2.

TABLE 1

<table>
<thead>
<tr>
<th>parameter</th>
<th>measured</th>
<th>calculated</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$g_m$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3. $A_V =$

4. ...................................................................................................................
   ...................................................................................................................
   ...................................................................................................................
   ...................................................................................................................

5. $A_V = (reduced \ R_L)$

6. $A_V = (reduced \ C_{bypass})$

Drawings for 3, 5, 6: (Draw in different colors for Vin and Vout)

(3) ———— (5) ————

(6) ————